WHAT IS CLAIMED IS:

1. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly and a common electrode line assembly on a first substrate, the gate line assembly comprising a plurality of gate lines and gate pads, the common electrode line assembly comprising common signal lines and common electrodes;

forming a gate insulating layer;

forming a semiconductor pattern;

forming an ohmic contact pattern;

forming a data line assembly and pixel electrodes, the data line assembly comprising a plurality of data lines, data pads, and source and drain electrodes, the pixel electrodes being connected to the drain electrodes while proceeding parallel to the common electrodes;

forming a passivation layer; and

etching the passivation layer and the gate insulating layer such that the gate pads and the data pads are exposed to the outside;

wherein the passivation layer and the gate insulating layer are etched after a second substrate is assembled to the first substrate, and the passivation layer and the gate insulating layer are exposed externally to the second substrate.

2. The method of claim 1, wherein the passivation layer and the gate insulating layer are exposed outside of the second substrate.

3. The method of claim 1, wherein the gate and the data pads is exposed

after injecting liquid crystal molecules in-between the first substrate and the second substrate facing each other, and sealing the gap between the first substrate and second substrate.

4. The method of claim 1, wherein the data line assembly, the pixel electrodes, the ohmic contact pattern and the semiconductor pattern are formed through a photolithography using one photoresist pattern of different thickness

wherein the photoresist pattern has a first portion placed between the source electrode and the drain electrode with a predetermined thickness, a second portion for forming the data line assembly and the pixel electrodes thicker than the first portion, and a third portion thinner than the first portion.

5. The method of claim 4, wherein the photoresist pattern is formed using a mask with thin films of different light transmission.

6. The method of claim 5, wherein the mask comprises a thin film with a light transmission of 20 to 50% corresponding to the first portion of the photoresist pattern, and a thin film with a light transmission of 3% or less corresponding to the second portion of the photoresist pattern.

7. The method of claim 4, wherein the photoresist pattern is made using a mask with a minute pattern, the minute pattern of the mask corresponding to the area between the source electrode and the drain electrode while bearing an opening width smaller than the resolution of a light exposing device.

8. The method of claim 7, wherein the minute pattern is either a slit pattern or a mosaic pattern.

9. The method of claim 7, wherein the opening width of the minute pattern

is 2μm or less.

10. The method of claim 1, wherein subsidiary data lines are formed at the step of forming the gate line assembly, and first contact holes exposing the subsidiary data lines are formed at the step of forming the gate insulating layer, the steps of forming the ohmic contact pattern, the semiconductor pattern and the first contact holes being made through a photolithography using one photoresist pattern of different thickness, the photoresist pattern having a first portion corresponding to the ohmic contact pattern and the semiconductor pattern with a predetermined thickness, a second portion thicker than the first portion, and a third portion corresponding to the first contact holes and thinner than the first portion.

11. The method of claim 10, wherein the pixel electrodes are formed in a linear shape while proceeding parallel to the common electrodes.

12. The method of claim 11, further comprising the step of forming one or more light interception patterns to be placed at the same plane as the gate lines with the same material such that each light interception pattern is separated from the gate line and positioned close to the neighboring subsidiary data line while proceeding parallel to the subsidiary data line.

13. The method of claim 12, wherein the pixel electrodes are partially overlapped with the light interception patterns.

14. The method of claim 12, wherein the pixel electrodes are spaced apart from the light interception patterns by a distance of 2μmor less.

15. The method of claim 10, further comprising the steps of:

forming a gate short circuit line that is connected to the gate pads;

forming a second contact hole at the gate insulating layer that exposes the gate short circuit line; and

forming a data short circuit line that is connected to the data pads, and is connected to the gate short circuit line through the second contact hole.

16. A liquid crystal display, comprising:

a first substrate;

a gate line assembly and a common electrode line assembly formed on the first substrate, the gate line assembly comprising a plurality of gate lines proceeding in the horizontal direction and gate pads connected to the gate lines, the common electrode line assembly comprising common signal lines proceeding parallel to the gate lines and common electrodes connected to the common signal lines while proceeding in the vertical direction;

a gate insulating layer covering the gate line assembly and the common electrode line assembly;

a semiconductor pattern formed on the gate insulating layer;

an ohmic contact pattern formed on the semiconductor pattern;

a data line assembly and pixel electrodes, the data line assembly comprising a plurality of data lines formed on the gate insulating layer and the ohmic contact pattern while crossing over the gate lines to form pixel regions, data pads connected to the data lines, source electrodes being parts of or branched from the data lines and drain electrodes separated from the source electrodes, the pixel electrodes connected to the drain electrodes at the pixel regions while proceeding parallel to the common electrodes;

a passivation layer covering the data line assembly and the pixel electrodes; and

a second substrate facing the first substrate;

wherein the gate insulating layer and the passivation layer exposed externally to the second substrate and the data pads are removed.

17. The liquid crystal display of claim 16, wherein the ohmic contact pattern has the same shape as the data line assembly and the pixel electrodes, and the semiconductor pattern has the same shape as the data line assembly and the pixel electrodes except for the area between the source and the drain electrodes.

18. The liquid crystal display of claim 16, further comprising subsidiary data lines placed at the same plane as the gate line assembly with the same material, and first contact holes formed on the gate insulating layer while exposing the subsidiary data lines.

19. The liquid crystal display of claim 18, wherein each pixel electrode is formed with two or more linear electrode portions, and each linear electrode portion is positioned close to the neighboring data line.

20. The liquid crystal display of claim 19, wherein both ends of the linear electrode portions are connected to each other such that the pixel electrode bears a ring shape.

21. The liquid crystal display of claim 20, further comprising one or more light interception patterns separated from the gate lines and positioned close to the subsidiary data lines while proceeding parallel to the subsidiary data lines.

22. The liquid crystal display of claim 21, wherein the pixel electrodes are

partially overlapped with the light interception patterns.

23. The liquid crystal display of claim 21, wherein the pixel electrodes are spaced apart from the light interception patterns by a distance of 2or less.

24. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly and a common electrode line assembly on a substrate including a display areas and a peripheral areas, the gate line assembly comprising a plurality of gate lines and gate electrode of the display areas, and gate pads of the peripheral areas, the common electrode line assembly comprising common signal lines and common electrodes of the display areas;

forming a gate insulating layer covering the gate line assembly exposing the portions of the gate pads;

forming a semiconductor pattern;

forming an ohmic contact pattern; and

forming a data line assembly and pixel electrodes, the data line assembly comprising a plurality of data lines, source and drain electrodes of the display areas, and data pads of the peripheral areas, the pixel electrodes being electrically connected to the drain electrodes while proceeding parallel to the common electrodes;

wherein a shadow frame having a first deposition blocking areais used to prevent the gate insulating layer from being deposited on the gate pads of the peripheral areas in the step of forming the gate insulating layer.

25. The method of claim 24, wherein the shadow frame has a second deposition blocking areato prevent the gate insulating layer, the semiconductor pattern,

or the ohmic contact pattern from being deposited on areas for the data pads of the peripheral areas.

26. The method of claim 24, wherein the steps of forming the data line assembly, the pixel electrodes, the ohmic contact pattern and the semiconductor pattern are made through a photolithography using one photoresist pattern of different thickness, the photoresist pattern having a first portion placed between the source electrode and the drain electrodewith a predetermined thickness, a second portion for forming the data line assembly and the pixel electrodes thicker than the first portion, and a third portion thinner than the first portion.

27. The method of claim 26, wherein the data line assembly, the ohmic contact pattern and the semiconductor pattern are formed through a photolithography using one mask.

28. The method of claim 27, wherein the steps of forming the gate insulating layer, the semiconductor pattern, the ohmic contact layer pattern, and the data line assembly comprise:

depositing the gate insulating layer, a semiconductor layer, an ohmic contact layer, and a conductor layer:

coating a photoresist layer on the conductor layer;

exposing the photoresist layer to light through the mask;

forming the photoresist pattern such that the second portion lies on the data line assembly by developing the photoresist layer;

forming the data line assembly, the ohmic contact layer pattern, and the semiconductor pattern respectively made of the conductor layer, the ohmic contact

layer and the semiconductor layer by removing a portion of the conductor layer under the third portion, the semiconductor layer and the ohmic contact layer thereunder, the first portion, the conductor layer and the ohmic contact layer under the first portion, and a partial thickness of the second portion; and

removing the photoresist pattern.

29. The method of claim 28, wherein the step of forming the data wire, the ohmic contact layer pattern and the semiconductor pattern comprises;

removing the portion of the conductor layer under the third portion by dry or wet etching to expose the ohmic contact layer;

dry etching the ohmic contact layer under the third portion, the semiconductor layer thereunder and the first portion to obtain the completed semiconductor pattern along with exposing the gate insulating layer under the third portion and the conductor layer under the first portion; and

removing the conductor layer under the first portion and the ohmic contact layer thereunder to complete the data wire and the ohmic contact layer pattern.

30. The method of claim 29, wherein the shadow frame is used to prevent the semiconductor layer, the ohmic contact layer, or the conductor layer from being deposited on the gate pad of the peripheral areas in the step of depositing the semiconductor layer, the ohmic contact layer, and the conductor layer.

31. The method of claim 30, wherein the photoresist pattern has a fourth portion placed on the gate pad portions, and having the thickness of the first, the second, or the third portion.

32. The method of claim 26, wherein a mask used for forming the

photoresist pattern has a first, a second, and a third part, the transmittance of the third part is higher than the first and the second parts, the transmittance of the first part is higher than the second part, the photoresist pattern is made of positive photoresist, and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the photoresist pattern in an exposing step.

33. The method of claim 32, wherein the first part of the mask includes a partially transparent layer.

34. The method of claim 32, the first part of the mask includes a plurality of slit patterns smaller than the resolution of the exposure device used in the exposing step.

35. The method of claim 26, wherein the first portion is formed by reflow.

36. The method of claim 24, further comprising the step of depositing a passivation layer;

wherein the shadow frame is used to prevent the passivation layer from being deposited on the peripheral areas having the gate and the data pads.